GaN-Based Permeable Base Transistor and Method of Fabrication

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RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/527,238, filed December 4, 2003, which is herein incorporated in its entirety by reference.

FIELD OF THE INVENTION

[0002] The invention relates to transistors, and more particularly, to permeable base transistors.

BACKGROUND OF THE INVENTION

[0003] There is increasing need for new devices that can operate at frequencies greater than 1 GHz. The wide bandgap semiconductor gallium nitride (GaN) has received much interest in the last decade as a material for high efficiency, high power microwave devices due to its high breakdown field and electron saturation velocity, and low thermal generation rate. Unfortunately, there is no native substrate on which to grow GaN device epilayers, hence the films are grown heteroepitaxially on sapphire or silicon carbide substrates.

[0004] Such growth results in films with considerable vertical threading dislocation densities that limit electron mobility in lateral devices such as metal semiconductor field effect transistors (MESFETs) or high electron mobility transistors (HEMTs). Yet the vertical mobility is enhanced. This physical attribute together with the material properties previously mentioned makes GaN a highly suitable material for a permeable base transistor (PBT).

[0005] The PBT is device very similar to the MESFET but with vertical transport instead of lateral, and has received much attention in the last quarter of a century due to its potential as a high power, high frequency, and high temperature-operating device. PBTs were suggested as early as 1964, and are typically fabricated using silicon, cobalt disilicide, gallium arsenide, silicon carbide, nickel phthalocyanine, and copper phthalocyanine.

[0006] Due to the early stage of development in the GaN growth and understanding of the material properties, PBTs fabricated with GaN have only recently been attempted. Reported modeling simulations of a GaN based PBT with a cut-off frequency (f_T) as high as 24.8 GHz and maximum frequency of oscillation (f_{max}) of 75.2 GHz. Such performance is relatively limited.

[0007] What is needed, therefore, techniques for making high power GaN PBTs using GaN.

SUMMARY OF THE INVENTION

[0008] One embodiment of the present invention provides an etched grooved GaN-based permeable-base transistor device. The device includes a GaN emitter region (e.g., having a thickness of about 6 to 10 μm) that is grown (e.g., on (0001) sapphire) using hydride vapor-phase epitaxy (HVPE). This emitter region may further include He implantation under base and collector contact pads to provide pad isolation (e.g., implant angle of about 7°). The device further includes a GaN base region (e.g., having a thickness of about 1 to 2 μm) that is grown on the GaN emitter region using molecular beam epitaxy (MBE). The device further includes a GaN collector region (e.g., having a thickness of about 0.1 to 0.3 μm) that has a plurality of collector fingers The collector region is grown on the GaN base region using MBE. In one such particular embodiment, the collector fingers have finger sidewall angles of about 80° to 85° for 1:1 and 1:3 finger spacing. In another particular such embodiment, the collector region has a collector pad region and a plurality of collector fingers, wherein the collector fingers have a first height in the collector pad region and a second height out of the collector pad region, with the first and second heights configured so as to prevent disconnect between the collector fingers and the collector pad

region. For instance, the difference in the first and second heights could be the thickness of one layer of collector pad metal.

[0009] Another embodiment of the present invention provides a method for fabricating an etched grooved GaN-based permeable-base transistor device. One such embodiment of the method includes seven mask levels, including: Level 1 - He implant mask; Level 2 - nitride isolation pad; Level 3 - collector ohmic pad mask; Level 4 - e-beam lithography of collector fingers for liftoff; Level 5 - base recess and metallization; Level 6 - emitter and device isolation etch, emitter ohmic; and Level 7 - microwave test pad metal deposition. Note that not all seven masks need to be used in practicing other embodiments of the present invention.

[0010] The features and advantages described herein are not all-inclusive and, in particular, many additional features and advantages will be apparent to one of ordinary skill in the art in view of the drawings, specification, and claims. Moreover, it should be noted that the language used in the specification has been principally selected for readability and instructional purposes, and not to limit the scope of the inventive subject matter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1a is a side and top perspective view of a GaN PBT device configured in accordance with an embodiment of the present invention.

[0012] Figure 1b is a vertical cross sectional view of the GaN PBT device shown in Figure 1a.

[0013] Figure 2a demonstrates the material structure of a GaN PBT device configured in accordance with an embodiment of the present invention.

[0014] Figure 2b illustrates various views of a GaN PBT device used to illustrate fabrication processes configured in accordance with an embodiment of the present invention.

[0015] Figures 3a through 7 illustrate a seven mask process flow for fabricating an GaN PBT and variations thereof in accordance with an embodiment of the present invention.

[0016] Figure 8 is a top plan view SEM picture of a completed GaN PBT device fabricated in accordance with an embodiment of the present invention.

[0017] Figure 9 (a and b) are SEM pictures showing a GaN PBT device fabricated in accordance with an embodiment of the present invention, with Figure 9a showing a 1:1 finger pitch, and Figure 9b a 1:3 finger pitch.

[0018] Figure 10 is a graph showing a I-V characteristic curve of a GaN PBT device fabricated in accordance with an embodiment of the present invention.

[0019] Note that the various features shown in the Figures are not drawn to any particular scale. Rather, the Figures are drawn to emphasize features and structure for purposes of explanation. The actual geometries and scale of the pertinent features and structure will be apparent in light of this disclosure.

DETAILED DESCRIPTION OF THE INVENTION

[0020] Embodiments of the present invention provide a design and method of fabrication of an etched grooved GaN-based permeable-base transistor structure. Process flow details regarding passivation, active region dry etching, and a mask set designed for PBT fabrication are disclosed. The mask set is configured to provide discrete PBT devices with a range of geometries for different frequency and power level operation, and high quality metal contacts to the various GaN layers.

[0021] One particular embodiment is fabricated using n-type GaN grown by hydride vapor phase epitaxy (HVPE) and molecular beam epitaxy on thick HVPE GaN quasi-substrates. The fabrication process employs isolation pads via helium (He) implantation and silicon nitride (SiN) deposition, as well as sub-micron chlorine-based high density inductively coupled plasma (ICP) etching of collector fingers patterned via e-beam lithography. Base Schottky contacts are deposited on the etched GaN layer prior to ohmic metal deposition so Schottky contacts on dry etched surfaces as well as low temperature annealed (0 - 500°C) Schottky and ohmic contacts are characterized for their performance.

[0022] The resulting high power GaN PBT device has a cutoff frequency f_T of about 134 GHz and a maximum frequency f_{max} of about 500 GHz. The device has a breakdown voltage of about 50V and a g_m of 70 mS/mm. Analysis of the device topology shows smooth etched finger structures and base layer surface with finger sidewall angles of about

80° to 85° for 1:1 and 1:3 finger spacing. Specific contact resistivities of about 3×10^{-6} $\Omega \bullet cm^2$ for the ohmic contacts were achieved with Ti/Al/Ni/Au metallization scheme. DC testing of these example devices show a current density J_S as high as 518 mA/mm^2, and a collector current I_C of about 140 mA/mm, both at V_{CE} of 5V and V_{BE} of +0.5V. The transconductance g_m achieved is about 111 mS/mm in the measured collector-emitter bias range. These actual results are comparable, within the measurement tolerance, to physics-based modeling results.

[0023] Other configurations will be apparent in light of this disclosure. In any such cases, a GaN PBT is provided that combines the high breakdown field of GaN and the good frequency response of a PBT. Applications for use include, for example, millimeter-wave power applications.

PBT Structure

[0024] Generally, there are two types of PBTs: etched groove and embedded or overgrown. In the case of etched groove, many submicrometer bases lay in etched grooves between ridge-like emitter contacts. In the case of embedded or overgrown, the base is completely buried inside the semiconductor lattice by epitaxial regrowth of the semiconductor. Embodiments of the present invention are directed to the etched groove type PBT.

[0025] The operation of the PBT is very similar to that of the MESFET except that the PBT is a vertical device and the MESFET is a lateral carrier device. In the PBT, the current flows perpendicular to the material surface. With this type of device, the thickness of the grown material layers can be altered to vary the device characteristics. In addition, the PBT is unipolar with a relatively short base length compared to the base length of a MESFET.

[0026] Figures 1a and 1b illustrate an etched groove PBT with metal contact configured in accordance with one embodiment of the present invention. To fabricate an etched groove PBT with suitable electrical characteristics, two conditions should be met: the spacing between metal fingers should be such that the two depleted zones meet (e.g., spacing between metal fingers smaller than 1 μm); and the leakage current of both base-collector and base-emitter Schottky diodes should be minimized. This requires a relatively

large Schottky barrier height (Φ_B >1 eV) on the material with which it is in contact. This submicrometer-periodicity Schottky-barrier grating is used to modulate the vertical flow of electrons.

[0027] As shown in Figures 1a and 1b, the top ohmic layer serves as the collector contact (on top of the device fingers). The bottom and middle ohmic layers serve as the emitter and base contacts, respectively, which are deposited in two separate etched regions. Since the gate length (l_g) is defined by the thickness of the Schottky metal in the base region, l_g can be realistically fabricated as smaller than 0.1 μm (the limit of most conventional transistors). Because of this, the effective channel length is mainly controlled by the depletion width towards collector and emitter.

[0028] The device was fabricated starting from a GaN quasi-substrates (e.g., 6 to 10 μm) grown on (0001) sapphire using a hydride vapor-phase epitaxy (HVPE) reactor. Note that this GaN quasi-substrate layer also serves as the emitter region for the PBT. In one embodiment, this layer is auto-doped n-type with a silicon (Si) carrier concentration of about 5 X 10^{18} cm^{-3}. Atomic force microscopy (AFM) studies on the GaN quasi-substrates show a step-flow growth mode with atomically smooth terraces or "fingers" of 0.2 μm width and step-height of 2 monolayers. RMS roughness of 0.45 nm was obtained over a 10 X 10 μm area.

[0029] The base and collector epilayers of this embodiment are 1.3 μm and 0.2 μm thick, respectively. The layers can be grown by plasma-enhanced molecular beam epitaxy (MBE) carried out, for example, in a Varian GenII system. Other such systems can be used here as well. Seamless epitaxy of GaN via MBE on GaN quasi-substrates can be achieved by growing the epilayers in group III-rich conditions. These base and emitter layers replicate the underlying GaN quasi-substrate layer without renucleation. The base and collector layers are doped with silicon (Si) to carrier concentrations of 5 X 10^{16} and 5 X 10^{18}, respectively.

[0030] When the PBT is in ON condition, the majority carriers flow from emitter (held at ground potential) to collector (biased at positive potential). Under normal operation, the Schottky barrier is reverse-biased by a negative base-to-emitter voltage. A voltage dependent depletion region forms beneath the Schottky barrier. This constricts the

effective area of the *n*-channel (reducing the depletion region on either side of the emitter finger), causing the channel to open and the collector current to vary with applied base bias.

[0031] In a PBT, the base bias induces a potential barrier under the collector. Near pinch-off, electrons that are injected from the emitter are accelerated by the collector bias, and pass across the potential barrier. At higher collector biases, the thermionic emission current rises exponentially with applied collector bias eventually becoming space charge limited, resulting in a triode mode device operation, where the collector current does not saturate at high collector voltages.

[0032] When a negative bias is applied to the collector, the depletion region expands and current flow through the channel is restricted. This will ultimately result in pinch off of the channel, and turn off of the PBT. Pinch off can be approximated using the equation:

$$V=\frac{1}{2}\frac{q\,N\,a^2}{\varepsilon_r\,\varepsilon_0}$$

where q is the charge of an electron, a is the channel thickness (or, in the case of a PBT, half the width of 1 finger), ε(r) is the relative permittivity of the material, and ε(0) is the permittivity of vacuum.

Fabrication Methodology

[0033] Figures 3a through 7 demonstrate a process flow for the fabrication of a GaN PBT in accordance with one embodiment of the present invention. This process flow includes all steps required to fabricate the device, as well as the design of a photolithography mask set drawn using AutoCAD. Various process alternatives are also provided.

[0034] The GaN PBT, because it is based on vertical transport, has three distinctly doped layers versus the two of lateral transistor devices for the metal contacts and the device itself to perform optimally. The material structure to be employed in the GaN PBT, in accordance with one embodiment of the present invention, is shown in Figure 2a.

[0035] Due to the lattice mismatch of GaN grown on sapphire or SiC, the bottom n^+ layer is deposited thick (e.g., n^+ 5 x 10^{18} cm^{-3}, HVPE) to keep the vertical threading dislocations minimal. The layer structure is chosen because the heavily doped regions will

be used for ohmic contacts and the lightly doped region will be used for a Schottky contact to adequately pinch off for a given range of high frequency operation. The desired blocking voltage of the transistor determines the thick n- region. The final structure will look similar to that shown in Figure 1b, where the material layers are the same as in Figure 2a.

[0036] Note that a full PBT will have a plurality of the collector fingers, and is this particular case. Only three are shown in Figure 1b for the purpose of illustration. In one particular embodiment, the full PBT device has 20 collector fingers, each surrounded by two base regions to control the width of the channel, as shown in Figure 1b. It will be appreciated that, in developing a process for a PBT device, it is necessary to have tolerances to variability in the semiconductor material characteristics and fabrication process. Some tolerances that are used herein are passivation layers, implantation, and pre-metal deposition treatments.

[0037] When referring to example embodiments of the PBT process described herein, the following views shall be discussed and are illustrated in Figure 2b: view 1 is the overall top view; view 2 is the cross section through the collector RF probe pad; view 3 is the cross section through the collector ohmic pad; view 4 is the cross section through the base collector fingers; and view 5 is the cross section through the base RF probe pad.

[0038] This is a seven-mask process flow that is the baseline for all of the subsequent versions. Various modifications and details not included in this version will be apparent in light of this disclosure.

[0039] This particular embodiment begins with the HVPE growth of 10 μm of heavily doped (e.g., $2x10^{18}$ cm^{-3} to $5x10^{18}$ cm^{-3}) n-GaN followed by 2 μm of MBE grown, lightly doped (e.g., $2x10^{16}$ cm^{-3} to $5x10^{16}$ cm^{-3}) n-GaN and 0.3 μm of MBE grown, highly doped (e.g., $2x10^{18}$ cm^{-3} to $5x10^{18}$ cm^{-3}) n-GaN. The silicon nitride deposition (to be discussed in turn) is to passivate the sidewalls of the collector fingers to prevent shorting of the base to the collector if metal accidentally deposits on the sidewalls.

[0040] The mask levels for this example process are shown here in Table 1:

Level 1	He implant mask
Level 2	Nitride isolation pad

Level 3	Collector ohmic pad mask
Level 4	E-beam lithography of collector fingers for liftoff
Level 5	Base recess and metallization
Level 6	Emitter and device isolation etch, emitter ohmic
Level 7	Microwave test pad metal deposition

Table 1

[0041] The process flow will now be discussed in steps, and with reference to the Figures 3a through 7. Note that the following steps are not necessarily intended to implicate any rigid order of performance, and other embodiments may have the steps performed in a different order, with a similar end product produced.

[0042] Step 1: Perform RCA wafer clean. The purpose of the RCA wafer clean is to remove organic contaminants (e.g., dust particles, grease or silica gel) from the wafer surface, as well as any oxide layer that may have built up, and any ionic or heavy metal contaminants.

[0043] Step 2: Open windows for helium (He) implantation using optical lithography. Due to the fact that the PBT is a "normally-on" device, the semiconductor material is conducting by default. Thus, an insulating layer is used to isolate the pads from the device. In this particular embodiment, the insulating layer is provided with He implantation. Figure 3a shows the optical lithography for He implantation of this step. As can be seen, the photo resist (PR) is shown is each of the views in locations where no He implantation is desired. In one particular embodiment, the wafer is patterned with about 9 μm photo resist for the He implantation.

[0046] Step 3: Perform He^{2+} implantation at about 250 keV, 1.35 μm isolation depth (determined from a TRIM calculation). Figure 3b shows the locations of He implantation with the diagonal striping. In one particular embodiment, a dose of about 1×10^{15} cm^{-3} was targeted with an acceleration voltage of 180 keV at an implant angle of 7°. With these parameters, TRIM simulations estimated an implant depth of about 2 μm.

[0047] Step 4: Strip the photo resist mask. The resulting structure after stripping is shown in Figure 3c.

[0048] Step 5: Open windows for thin, high quality silicon nitride pad (SiN_x), about 1000-2000Å thick, using optical lithography. Figure 3d shows the optical lithography for the SiN_x pad of this step.

[0049] Step 5a: Perform deposition of high quality SiN_x pad, 1000-2000Å thick. This SiN_x layer serves as the second electrical isolation for the collector and base contact pads. Figure 3e shows the resulting structure after the SiN_x deposition of this step. In one particular embodiment, 1000 Å of high quality SiN_x pads were deposited on top of the He-implant region via plasma enhanced chemical vapor deposition (PECVD).

[0050] Step 5b: Perform lift-off of high quality silicon nitride pad, 1000-2000Å thick. Figure 3f shows the resulting structure after the SiN_x lift-off of this step, where all SiN_x deposited on top of photo resist is removed.

[0051] Step 6: Open windows for Ti metal pad using optical lithography. Figure 3g shows the optical lithography for the Ti pad of this step.

[0052] Step 6a: Perform Ti metallization. Figure 3h shows the resulting structure after the Ti metallization of this step. In one particular embodiment, Ti/Au (500Å/1000Å) collector metal pads are deposited using e-beam evaporation.

[0053] Step 6b: Perform lift-off of Ti metallization. Figure 3i shows the resulting structure after the Ti metallization lift-off of this step, where all Ti deposited on top of photo resist is removed.

[0054] Step 7: Perform E-beam lithography of collector fingers and for self-aligned base recess and metallization. Figure 3j shows the E-beam lithography of the collector fingers of this step. In one particular embodiment, the wafer is patterned with e-beam lithography using PMMA photo resist (about 0.14 μm) for the metallization of the collector fingers.

[0055] Step 7a: Perform ohmic metallization of collector. Prior to metallization, a 1 minute HCl:DI $H_2 0$ (1:1) dip is used for removing contaminants on the semiconductor surface. Although not mentioned in other steps, this can beneficially be used for all metal depositions on semiconductor material. Figure 3k shows the resulting structure after the Ti/Ni metallization of this step. In one particular embodiment, the metal scheme used for the collector fingers is Ti/Ni with thicknesses of 100Å and 400Å, respectively. With this arrangement, Ti acts as the metal contact, while Ni serves as the base shallow etch mask.

[0056] Step 7b: Perform lift-off of ohmic metallization of collector. Figure 3m shows the resulting structure after the Ti/Ni metallization lift-off of this step, where all Ti/Ni deposited on top of photo resist is removed. In one particular embodiment, each collector finger is about 0.2 μm wide and 230 μm in length. Since only 200 μm of this length covers each finger active region of the device, the total finger area is 40 μm^2. Each device has 20 fingers either with a 1:1 pitch (evenly spaced) or 1:3 pitch.

[0057] Step 8: Open windows for a Ti cap in collector pad region using optical lithography. Figure 3n shows the optical lithography for the Ti cap of this step.

[0058] Step 8a: Deposit thin Ti cap in collector pad region again to prevent collector metal fingers from peeling upward and losing contact to the pad. Figure 3p shows the resulting structure after the Ti metallization of this step. In one particular embodiment, Ti/Au (500Å/1000Å) collector metal caps are deposited using e-beam evaporation.

[0059] Step 8b: Perform lift-off of the thin Ti cap in collector region. Figure 3q shows the resulting structure after the Ti metallization lift-off of this step, where all Ti deposited on top of photo resist is removed.

[0060] Step 9: Open windows for the base recess/metallization (collector lines are part of mask) using optical lithography. Figure 3r shows the optical lithography for the base recess/metallization of this step.

[0061] Step 9a: Perform a high density plasma etch to recess the base layer to n^- layer (e.g., about 0.5 μm). Figure 3s shows the resulting structure after the high density plasma etch in the base region of this step. In one particular embodiment, the wafer is etched using a custom-built inductively coupled plasma (ICP) etching system utilizing pure Cl_2 chemistry. Etching can be performed at a chamber pressure of about 3.8×10^{-3} torr, 350 W ICP power and about –400 V chuck bias with a ramp down to about –200V bias for the last minute of the etch. The ramp down etches a layer of material damaged by plasma leaving behind undamaged GaN for subsequent metal contact deposition. This etch-damage removal enables excellent ohmic electrical characteristics. Approximately 0.5 μm etch depth is achievable.

[0062] Step 9b: Perform conformal SiN_x deposition for spacer and sidewall passivation. This layer prevents shorting between the base and collector if metal accidentally deposits

on the finger sidewalls. Figure 3t shows the resulting structure after the SiN_x deposition for spacer and sidewall passivation of this step. In one particular embodiment, the conformal SiN layer is less than 500 Å.

[0063] Step 9c: Perform directional etch to remove SiN_x on parallel surfaces. Figure 3u shows the resulting structure after the directional etch for SiN_x removal of this step. In one particular embodiment, a directional reactive-ion etching (RIE) of the SiN planes parallel to the surface was used to expose the base layer between the fingers.

[0064] Step 9d: Perform base metallization (Pt/Ni). Figure 3v shows the resulting structure after the base metallization of this step. In one particular embodiment, the base contact was deposited using Ni/Pt/Au (Schottky contacts) having layers of thickness 100Å/400Å /100Å, respectively.

[0065] Step 9e: Perform lift-off of base metallization (Pt/Ni). Figure 3w shows the resulting structure after the base metallization lift-off of this step.

[0066] Note that a post Schottky deposition anneal is used to alloy the ohmic contacts. This is because the Schottky metal is deposited before the emitter ohmic metal. A low temperature anneal does not substantially alter the forward bias behavior of the Schottky contacts, but decreases the reverse leakage current. Further note that the Schottky contacts are the contacts in the base region). In one particular embodiment, an anneal for about 60 seconds at 500°C is used to maintain low reverse current leakage while providing low contact resistance.

[0067] Step 10: Open emitter etch/contact window using optical lithography. Figure 3x shows the resulting structure after the optical lithography for emitter etch of this step. In one particular embodiment, the wafer is patterned with a thick photoresist (e.g., about 4 μm) for a deep etch of 2 μm to 3 μm down to the emitter layer via ICP etching.

[0068] Step 10a: Etch emitter recess to bottom, HVPE n^+ GaN quasi-substrate layer (e.g., about 2.5 μm). Figure 3y shows the resulting structure after the etching of the emitter recess of this step.

[0069] Step 10b: Perform emitter ohmic metallization. Figure 3z shows the resulting structure after the emitter ohmic metallization of this step. In one particular embodiment,

the emitter ohmic contacts were deposited using a Ti/Al/Ni/Au metal scheme having thicknesses of 300Å /1500Å /400Å /1500Å, respectively.

[0070] Step 10c: Perform lift-off of emitter ohmic metallization. Figure 3aa shows the resulting structure after the emitter ohmic metallization of this step.

[0071] Step 11: Open windows for RF test pad metallization using optical lithography. Figure 3bb shows the resulting structure after the optical lithography of this step.

[0072] Step 11a: Deposit RF test pad metal. Figure 3cc shows the resulting structure after the deposition of test pad metal of this step. In one particular embodiment, this metal includes an adhesion layer (e.g., titanium or nickel) and a thick gold (Au) capping layer, since Au is a good microwave conductor and prevents oxidation.

[0073] Step 11b: Perform lift-off RF test pad metal. Figure 3dd shows the resulting and final structure after the RF test pads liftoff of this step.

Variations on Fabrication Methodology

[0074] A first variation on the PBT fabrication methodology deals with the deposition of the SiN_x in step 5. In more detail, a conformal deposition of SiN_x over the entire wafer followed by photo resist patterning and wet chemistry etch to remove the SiN_x from the unwanted areas may be more desirable, since SiN_x is sometimes difficult to remove via liftoff. In this case, the SiN_x is about 1000Å thick, and the wet chemical etch will provide a shallow slope on the sidewalls which will ensure metal continuity from the collector fingers to the contact pad. In addition, the metal pad on top of the collector region can be altered to Ni/Pt because of the new Schottky metal on the collector fingers.

[0075] The electron beam lithography can also be changed, to provide a second variation. In particular, instead of opening up windows for the fingers and depositing metal as previously described in steps 7 through 7b, a large window can be opened. For example, Figure 4 shows the e-beam lithography for opening a large base window in accordance with one such embodiment of the present invention. This window would be used for base recess and metallization as well as collector finger metallization. This will ensure that the metal on the collector fingers is not very thick, thus minimizing the chance of connection between the various fingers.

[0076] Following base recess, all steps would be similar to those previously discussed until step 9d, where the Schottky metal deposited would be the metal for both the base region and collector fingers. The Schottky metal would be feasible as the collector metal because of ballistic electrons that could pass the potential barrier. In addition, the Ti capping layer on the collector contact in steps 8 through 8b can be omitted, in this particular variation.

[0077] In a third variation of the fabrication process, a "0" level Ti/Pt layer can be used. In more detail, note that the first layer (step 3) is a He implantation, which requires alignment for further steps in the process. In particular, implanted He areas are not distinguishable under optical alignment. For this reason, a "0" level mask for subsequent optical and electron beam alignment was added. The metal to be used for enabling optical alignment is titanium (Ti) followed by platinum (Pt). In one such embodiment, this "0" level mask is a Ti/Pt layer of about 200-500/1500Å, respectively. These metals are chosen because of Ti's good adhesion to GaN and Pt is a good alignment metal for e-beam writers (because it is high Z). Crosses for optical alignment and squares for e-beam alignment are thus provided.

[0078] The thick Pt was found to work best for this e-beam writing system. Also, it was found that the He^{2+} implantation given in step 3 would penetrate the photo resist about 3.50 μm based on a TRIM calculation of $R_P + \Delta R_P$ (the ion range and range straggling). This shows that a thick resist, such as AZ4620, is needed. In addition, the SiN_x etch can be done via a wet chemistry of NH_4F, which will leave a shallow slope on the nitride walls due to the slow etching and isotropy characteristic of wet chemistry etches. The e-beam photo resist, PMMA, is not intended to be a dry etch mask and for this reason, cannot be used as previously given in step 7. For this reason, only the collector fingers shall be opened.

[0079] In one such particular embodiment for high power operation, 20 fingers could be used. These fingers shall be 40 – 200 μm long and varying width (0.15 – 0.3 μm). The metal on top of these fingers can be, for example, Schottky, Ni/Pt/Ni (200/500/500 Å), where the final Ni layer is used as an etch mask since it was found to withstand a chlorine etch well. This is followed by the base etch similar to step 9. The settings of this etch

shall be ICP, ~0.43 μm in depth using pure Cl_2 chemistry, 400W ICP power, and 200eV ion energies. The low bias voltage is used to provide a slow and accurate etch depth. The structure resulting from the base etch following collector metal deposition (with photo resist) is shown in Figure 5a. The decreased etch depth (0.43 μm) is due to an additional etch step that is needed and will be described next.

[0080] A base metal deposition as given in step 9b isolates the base metal from the GaN material on the sides of the collector fingers so an additional etching after the SiN_x deposition is needed to expose the sidewalls of the collector fingers, and to allow better base metal contact and, therefore, better base voltage control of the collector current resulting in higher transconductance in the device. This deposited SiN_x is, for instance, less than 500Å via PECVD. This thickness is decreased since the minimum base region width is 1500Å and 1000Å of SiN_x on both sides would completely close the base region. This additional etch is a two-stage etch.

[0081] First, a $CH_4 - O_2$ mix is used via RIE to directionally remove the SiN_x since Cl_2 has a much faster etch rate on GaN than on SiN_x. Following SiN_x removal, an ICP base etch for collector finger contact will be used to etch the GaN 0.07 μm as shown in Figure 5b. The 0.07 μm depth is exactly the thickness of the subsequent metal deposition to prevent shorting of any metal that accidentally deposits on the sidewalls or in case the metal deposition is slightly thicker than expected. After this additional base etch for collector finger contact, the base is metallized with Ni/Pt (300/400 Å). Following this, all steps can be as previously discussed.

[0082] A fourth variation of the fabrication process includes the initial deposition of Ti/Al/Pt alignment markers. The addition of Al is to create an ohmic contact at the first layer for ohmic circular transmission line measurement (CTLM) and Schottky diode test structures that will be employed since the e-beam writer cannot write large areas during definition of the collector regions (otherwise, the first ohmic deposition). The addition of Al will not affect the e-beam alignment with the thick Pt (e.g., 1500 Å) deposited. He implantation under both base and collector contact pads is used due to the high conductivity of the material. This is shown in Figure 6a. The placement of the e-beam alignment markers is also given. Each alignment box is 4 μm x 4 μm. Note that they are

75 μm from the region to be written, due to the stringent requirements of the ebeam writing tool.

[0083] The first SiN_x deposition is similar to previous versions with the exception that it is now included under the base contact pad (as well as the collector pad) as shown in Figure 6b. This is a double safeguard for pad isolation. Now referring to Figure 6c, note that the metal deposition shown on the collector pad is altered. Ni and Pt are both high stress films, so Ti/Au was chosen as a replacement since Ti is low stress and Au prevents oxidation to underlying metals. In one particular embodiment, these are deposited at 500/1000 Å, respectively.

[0084] Collector fingers were also changed from Schottky to ohmic since collector and base metals were no longer to be deposited simultaneously. The new metal scheme is Ti/Ni (100/400Å). Process tests support the use of a thicker Ni layer and removal of the Al layer and are the reason for this increase in thickness. This thin metal is the maximum thickness allowed with the thin (e.g., 1500Å) e-beam resist needed for fine features (e.g., 0.15 μm). Following this metal liftoff, SiN_x is deposited (as previously described with the two stage etch).

[0085] After the base metallization, the emitter is etched. This requires a thick resist of, for instance, AZ4620 of about 4 μm. Dimensions of the emitter etch are given in Figure 6d, and the final device structure is shown in Figure 6e.

[0086] A fifth variation of the fabrication process includes a modification to the silicon nitride pad deposited in steps 5, 5a, and 5b. In this alternative embodiment, the SiN_x pad is square such that, the He implanted region will extend out to the collector fingers, and no SiN will be under the fingers. This will reduce the difference in height between the fingers in the collector pad region (e.g., view 3 of Figure 2b) relative to the height of the fingers out of the collector pad region (e.g., view 4 of Figure 2b), which helps to prevent the metal fingers from disconnecting from the collector pad due to a significant difference in height. One such alternative embodiment is shown in Figure 7, where there is only a layer of titanium under the fingers at the collector pad region (and no SiN layer). Thus, the height difference of the collector fingers in the collector region and the collector fingers out of the collector region is about one layer of titanium.

[0087] Figure 8 shows a top view SEM picture of a completed PBT device configured in accordance with the present invention. As can be seen, high accuracy in the alignment of the different mask layers was achieved since the devices were processed with an optical lithography alignment tolerance in the order of 1.5 μm. This tolerance is much smaller than the usual limit for this technique.

[0088] Figure 9 shows detailed SEM images of the collector finger of two different devices, with device (a) having 1:1 finger pitch and device (b) having 1:3 finger pitch. One half the finger width (0.2um/2) is the effective device channel and the base contact thickness (600Å) is the equivalent gate length. Note that these values are very small when compared to the conventional FET device features. Further note that a ramp down from –400V bias to –200V bias during the etch step produced a fairly smooth etched base surface. A finger sidewall angle of approximately 85^{o} was achieved, which is highly anisotropic. A nickel metal layer thickness of 400Å acted as an excellent etch mask as can be appreciated by the uniform morphology of the finger structures.

[0089] Probing of the various CTLM test structures shows ohmic metal contacts which have specific contact resistivity, ρ_c, of about $3 \times 10^{-6}\ \Omega\bullet cm^2$, which is an indication of the excellent contact quality.

[0090] The DC characteristic curve of a device with 1:1 finger pitch is shown in Figure 10. The output characteristics have been measured for an applied base-emitter bias V_{BE} ranging from +0.5 V to –1.0 V. The collector-emitter voltage V_{CE} is in the 0 V to 5.5 V range. From the plot, it is evident that the base voltage controls the output current I_C, showing transistor action. For V_{CE} = +5.0 V and V_{BE} = +0.5V, a current density J_C of up to 520 mA/mm^2 is achieved. DC testing of the devices shows good base control (modulation of I_{CE}), and current densities of up to 450 mA/mm^2 were achieved for a V_{CE} of 5.0V.

[0091] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.